

REMARKS

Claims 1 - 4 are presently pending in the application.

I. Claim Rejection -- 35 U.S.C. § 102(b)

Claims 1 - 4 stand rejected as allegedly being anticipated by U.S.P. No. 5,602,509 (“Kimura”). For the following reasons, this rejection is respectfully traversed.

Claim 1

Independent claim 1 recites (among other things) two input voltages being supplied to the circuit, the circuit having one output terminal for a subtractor and one output terminal for an adder, respectively. The instant invention provides a subtractor/adder circuit, wherein both a subtractor output voltage (V) and an adder output voltage (VS) may be output simultaneously. That is, the inputs and outputs have the same attribute of voltage. The circuit of the present invention is a voltage input / voltage output circuit. It is at least these features that are altogether absent in the prior art relied upon in the grounds of rejection.

The grounds of rejection compare the Operational Transconductance Amplifier (“OTA”) of the Kimura reference to the circuit of the instant invention. The grounds of rejection specifically point to Figs. 1 and 3 of the Kimura reference. However, the comparison of the OTA to the instant application is inapposite, as explained below.

An OTA is a voltage input / current output circuit that constitutes a voltage-to-current conversion circuit. That is, the output signal in the Kimura reference is a current output. Stated differently, an OTA does not have a voltage output.

In a voltage-to-current conversion circuit (such as the Kimura reference), it is inherent that an output current varies linearly in accordance with respect to a differential input voltage. Therefore, in the voltage-to-current conversion circuit, if the output current which corresponds to the input differential voltage is converted to a voltage, for example (by using an external circuit), it is possible to use the circuit as a subtractor. However, the circuit of Kimura does not have a current-to-voltage conversion circuit. Additionally, the circuit of the Kimura reference does not have an adder circuit and a voltage output for providing an addition result.

In contrast, the instant invention provides a subtractor/adder circuit. In the present invention, it is possible to output both a subtractor output voltage (V) and an adder output voltage (VS) *simultaneously*, in the same circuit. That is, the inputs and outputs have the same quality -- voltage. The circuit according to the present invention is a voltage input / voltage output circuit that, as an operational circuit, is naturally required to further possess linear outputs.

While the circuit of the Kimura reference and the circuit of the instant invention are both voltage input circuits (thus requiring linearity) they are not both voltage output circuits. The structures of the two circuits may appear slightly similar, but the actual circuit structures and functions thereof differ greatly from each other.

Accordingly, in light of the features of the instant invention that are altogether absent in the prior art relied upon in the grounds of rejection, the Examiner is respectfully requested to reconsider and withdraw this anticipation rejection.

AMENDMENT UNDER 37 C.F.R. § 1.114(c)
Application No. 09/940,472

Attorney Docket No. Q65962

Claims 2 - 4

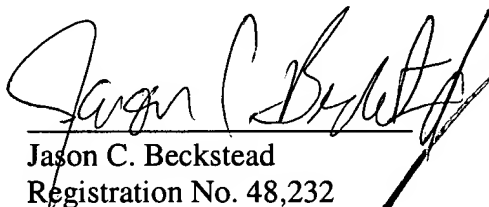
Claim 2 depends from claim 1 and is therefore averred to be patentable at least by virtue of its dependency.

Claim 3 is averred to be patentable at least for reasons analogous to those reasons finding claim 1 patentable. Similarly, claim 4 depends from claim 3 and is therefore averred to be patentable at least by virtue of such dependency.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,


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